Exhibit C

Office Action Summary	Application No. 15/820,076	Applicant(s) LEE ET AL.
	Examiner MICHAEL SUN	Art Unit 2184 / AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *11/21/2017*.
  ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☒ Claim(s) *1* is/are pending in the application.
  5a) Of the above claim(s) _____ is/are withdrawn from consideration.
6) ☐ Claim(s) _____ is/are allowed.
7) ☒ Claim(s) *1* is/are rejected.
8) ☐ Claim(s) _____ is/are objected to.
9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined <u>allowable</u>, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10) ☐ The specification is objected to by the Examiner.
11) ☒ The drawing(s) filed on *11/21/2017* is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  Certified copies:
    a) ☐ All   b) ☐ Some** c) ☐ None of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. _____.
    3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
  Paper No(s)/Mail Date _____.
3) ☐ Interview Summary (PTO-413)
  Paper No(s)/Mail Date. _____.
4) ☐ Other: _____.

Application/Control Number: 15/820,076   Page 2

Art Unit: 2184

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Status of the Application

This Office Action is in response to Applicant's Continuation filed on 11/21/2017.

Claim 1 is pending for this examination.

Obvious-Type Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine

grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible

harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where

the conflicting claims are not identical, but at least one examined application claim is not

patentably distinct from the reference claim(s) because the examined application claim is either

anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*,

140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d

2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van

Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619

(CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may

be used to overcome an actual or provisional rejection based on nonstatutory double patenting

provided the reference application or patent either is shown to be commonly owned with the

examined application, or claims an invention made as a result of activities undertaken within the

Application/Control Number: 15/820,076   Page 3
Art Unit: 2184

scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination

under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP

§§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor

to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR

1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used.

Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the

form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or

PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely

online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-

processed and approved immediately upon submission. For more information about eTerminal

Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as

being unpatentable over claims 1-22 of copending Application No. 15/426,064, now US Patent

No. 9,824,035; claims 1-20 of copending Application No. 14/846,993, now US Patent No.

9,563,587; and claims 1-20 of copending Application No. 13/952,599, now US Patent No.

9,128,632. Although the conflicting claims are not identical, they are not patentably distinct

from each other because claim 1 of instant Application, respectively contains every element of

claims 1-22 of copending Application No. 15/426,064, now US Patent No. 9,824,035; claims 1-

20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of

Application/Control Number: 15/820,076   Page 4

Art Unit: 2184

copending Application No. 13/952,599, now US Patent No. 9,128,632, as listed below, and as

such anticipate the claims of the copending application:

Claims	Instant Application	Claims	copending Application No. 13/952,599, now US Patent No. 9,128,632
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus; a module control device mounted on the module board and configured to receive command signals for a first operation via the set of control/address signal lines and to output module command signals and module control signals in response to the command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock, and to perform the first operation in	Independent claim 1	A memory module to operate in a memory system with a memory controller, the memory system operating according to a system clock, the memory system including a memory bus coupling the memory module to the memory controller, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module control device to receive memory command signals from the memory controller and to output module command signals and module control signals in response to each of the memory command signals; memory devices organized in groups, each group including at least one memory device, the memory devices receiving the module command signals from the module control device and performing one or more memory operations in accordance with the module command signals; and a plurality of buffer circuits to receive the module control signals, each respective buffer

Application/Control Number: 15/820,076   Page 5

Art Unit: 2184

	response to the module command signals, the memory' devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and. a respective set of memory devices, and configured to receive the module control signals and the module clock, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock, wherein the data path corresponding to the each data signal line includes a tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module		circuit corresponding to a respective group of memory devices and coupled between the respective group of memory devices and a respective set of the plurality of sets of data/strobe signal lines, the respective buffer circuit including data paths for communicating data between the memory controller and the respective group of memory devices, the data paths being controlled by at least one of the module control signals; and wherein the plurality of buffer circuits are distributed across a surface of the memory module in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines such that each module control signal arrives at the plurality of buffer circuits at different points in time, and wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.

Application/Control Number: 15/820,076   Page 6

Art Unit: 2184

	control signals.		
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 13/952,599, now US Patent No. 9,128,632, and as such would be rendered obvious over the already allowed claim language of copending Application No. 13/952,599, now US Patent No. 9,128,632.		

Likewise, the dependent claims of the above cited independent claims carry similar limitations to each other respectively.

Claims	Instant Application	Claims	copending Application No. 15/426,064, now US Patent No. 9,824,035
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective signal lines in the memory bus;

a module control device mounted on the module board and configured to receive command signals for a first operation via the set of control/address signal lines and to output module command signals and module control signals in response to the command signals, the module | Independent claim 1 | A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective data/strobe signal lines in the memory bus;

a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address signal lines and to produce module command signals and module control signals in response to the memory |

Application/Control Number: 15/820,076   Page 7

Art Unit: 2184

	control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock, and to perform the first operation in response to the module command signals, the memory' devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and. a respective set of memory devices, and configured to receive the module control signals and the module clock, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module		command signals; and memory devices mounted on the module board to perform a first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines; and a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit providing data paths between a respective set of the data/strobe signal lines and a respective set of the plurality of sets of memory' devices, the each respective buffer circuit including logic that responds to the module control signals by enabling a subset of the data paths for transmitting data and strobe signals corresponding to the first memory operation between the respective set of the data/strobe signal lines and the corresponding set of the plurality of sets of memory devices, wherein the logic is further configured to obtain timing information based on signals received by the each respective buffer circuit during a second memory operation prior to the first memory

Application/Control Number: 15/820,076   Page 8

Art Unit: 2184

	clock, wherein the data path corresponding to the each data signal line includes a tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.		operation and to control timing of the data and strobe signals on the subset of the data paths in accordance with the timing information.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 15/426,064, now US Patent No. 9,824,035, and as such would be rendered obvious over the already allowed claim language of copending Application No. 15/426,064, now US Patent No. 9,824,035.		

Likewise, the dependent claims of the above cited independent claims carry similar

limitations to each other respectively.

Claims	Instant Application	Claims	copending Application No. 14/846,993, now US Patent No. 9,563,587
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus;	Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board including edge connections for connecting to respective ones of the signal lines in the memory bus;

Application/Control Number: 15/820,076   Page 9

Art Unit: 2184

	a module control device mounted on the module board and configured to receive command signals for a first operation via the set of control/address signal lines and to output module command signals and module control signals in response to the command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock, and to perform the first operation in response to the module command signals, the memory' devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and. a respective set of memory devices, and configured to receive the module control signals and the module clock,		memory devices mounted on the module board, including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines; buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit being coupled between a respective set of the data/strobe signal lines and a corresponding set of memory devices; and a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address signal lines and to control the memory devices and the buffer circuits in response to the memory command signals; wherein the each respective buffer circuit is configured to respond to one or more first control signals from the module control device by receiving write data/strobe signals from the respective set of data/strobe signal lines and transmitting the write data/strobe signals to the corresponding set of memory devices during a memory write operation;

Application/Control Number: 15/820,076   Page 10

Art Unit: 2184

	the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock, wherein the data path corresponding to the each data signal line includes a tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.	wherein the each respective buffer circuit is further configured to respond to one or more second control signals from the module control device by receiving read data/strobe signals from the corresponding set of memory devices and transmitting the read data/strobe signals to the memory controller via the respective set of data/strobe signal lines during a memory read operation subsequent to the memory write operation; and wherein the each respective buffer circuit is further configured to time the transmission of the read data/strobe signals during the read operation based on timing information derived from receiving the one or more first control signals and the write data/strobe signals during the write operation.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 14/846,993, now US Patent No. 9,563,587, and as such would be rendered obvious over the already allowed claim language of copending Application No. 14/846,993, now US Patent No. 9,563,587.	

Likewise, the dependent claims of the above cited independent claims carry similar

limitations to each other respectively.

Allowable Subject Matter

Claim 1 is allowed.

Application/Control Number: 15/820,076   Page 11

Art Unit: 2184

The following is an examiner's statement of reasons for allowance:

Prior art teaches memory module systems arranged into respective groups of memory

devices, memory module systems with buffered memory modules, and memory module systems

that implement delays for transmitting signals to the memory devices of each module, however,

the prior art does not fairly teach or suggest, individually or in combination, a memory module

system with a plurality of buffers mounted in positions corresponding to the respective sets of

data / strobe signal lines, each buffer providing data paths between the data / strobe signal lines

and a set of memory devices and including logic that responds to control signals by enabling the

data paths corresponding to memory operations between the data / strobe signal lines and the

memory devices, wherein the logic is configured to obtain timing information based on signals

received by the buffers during a second memory operation prior to the first memory operation

and to control timing of the data and strobe signals on the data paths in accordance with the

obtained timing information as claimed. These limitations find support in Applicant's

Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the

above recited combination.

As allowable subject matter has been indicated, applicant's reply must either comply with

all formal requirements or specifically traverse each requirement not complied with. See 37

CFR 1.111(b) and MPEP § 707.07(a).

Contact Information

Application/Control Number: 15/820,076   Page 12
Art Unit: 2184

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to MICHAEL SUN whose telephone number is (571)270-1724.

The examiner can normally be reached on Monday-Thursday 6:45am-4:45pm.

Examiner interviews are available via telephone, in-person, and video conferencing using

a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is

encouraged to use the USPTO Automated Interview Request (AIR) at

http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application

Information Retrieval (PAIR) system. Status information for published applications may be

obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL SUN/

Primary Examiner, Art Unit 2184